ABSTRACT OF THE INVENTION

A data I/O system includes first and second function blocks
connected to a system bus, which allows the function blocks to

5   communicate with a processor. Each function block includes a D/A
converter for outputting an analog signal and a waveform
generator that provides a digital signal to the D/A converter.
The waveform generator includes a memory control circuit and
an address generation circuit. The memory control circuit has

10   an address register and a data register, both of which are
connected to the system bus, and a memory connected to the address
register and the data register. The address generation circuit
is connected to the address register and includes a control
register, an up-down counter, and a comparator. The address

15   generation circuit repetitively provides a circulating address
signal to the address register. The function blocks relieve the
processor of some of its processing load, but do not require
additional I/O port addresses of the system.